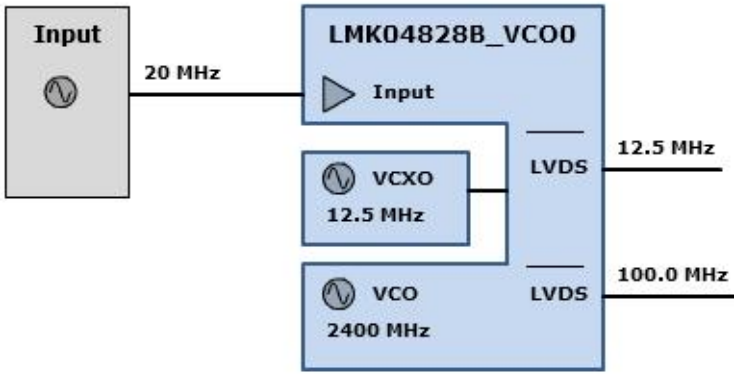
WEBENCH® Clock Architect

Project Report

Project: 5352910/34 Project 34 - [LMK04828B_VCO0]
Created: 5/7/19 12:56:36 AM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	100	LVDS	1
fixed1	12.5	LVDS	1

Options

Name	Design Value
Automatically Select Input Frequencies	No
Part Filter	LMK04828

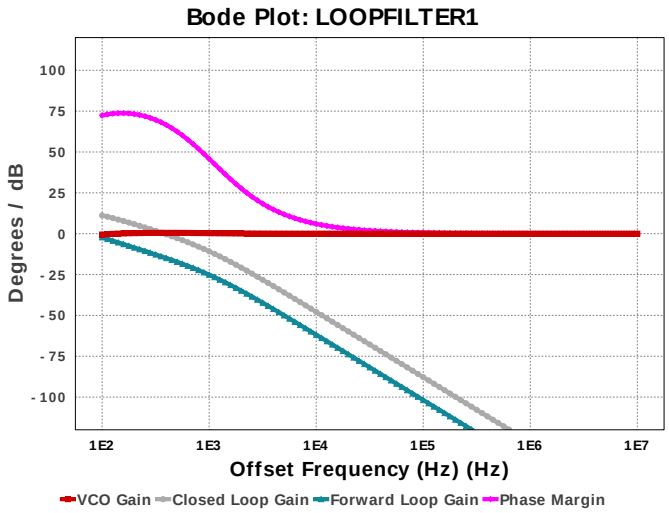
Properties

Name	Design Value
External Sources	VCXO(1)
Total BOM Cost	$16.2
Total Current	245.8 mA
Total Footprint	211.0 mm^2

User ID = 5352910
Design Id = 57
Device = LMK04828B_VCO0
Created = 5/7/19 12:56:36 AM

WEBENCH ® Clock Design Report

Loop Filter: LMK04828B_VCO0 LOOPFILTER1



Preferences

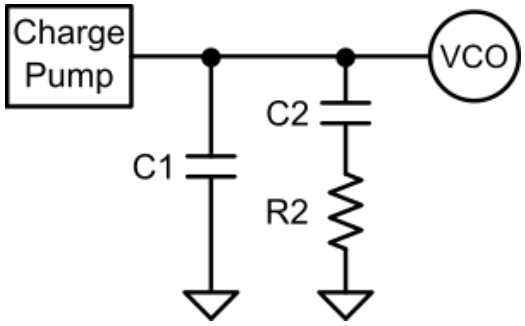
Name	Design Value
Filter Type	Passive
Filter Order	2nd Order
Op Amp Gain	1.00
Charge Pump Gain	0.45 mA
VCO Gain	0.002 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	12.50 MHz
Phase Det. Frequency	2.50 MHz
Filter type	designed
Brickwall Bandwidth	0.07844852583841189 kHz
Delta Sigma Order	0
Randomization Factor	0.0 %
PLL Whole Part	5
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

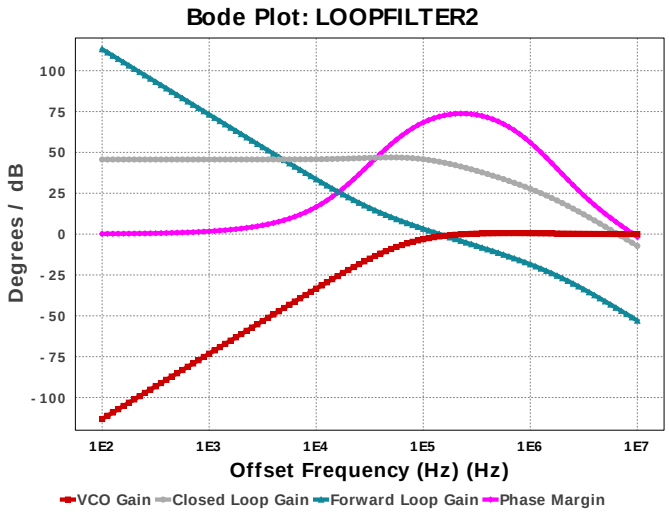
Name	Design Value	Forced	Actual Value
Loop Bandwidth	0.075 kHz	N	0.078 kHz
Phase Margin	70.00 deg	N	70.272 deg
T3/T1Ratio	0.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.262

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	56.00 nF	N	N
C2	2700.00 nF	N	N
C3	Open	N	N
C4	Open	N	N
R2	2.70 kohms	N	N



Loop Filter: LMK04828B_VCO0 LOOPFILTER2



Preferences

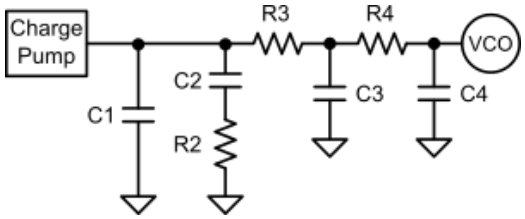
Name	Design Value
Filter Type	Passive
Filter Order	4th Order
Op Amp Gain	1.00
Charge Pump Gain	3.20 mA
VCO Gain	8.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	2400.00 MHz
Phase Det. Frequency	12.50 MHz
Filter type	designed
Brickwall Bandwidth	142.04117594472584 kHz
Delta Sigma Order	0
Randomization Factor	0.0 %
PLL Whole Part	96
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	122.733 kHz	N	142.041 kHz
Phase Margin	70.00 deg	N	71.985 deg
T3/T1Ratio	50.00 %	N	2.481 %
T4/T3Ratio	50.00 %	N	29.575 %
Gamma	0.24	N	0.382

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.015 nF	N	N
C2	1.80 nF	N	N
C3	0.01 nF	Y	N
C4	0.01 nF	Y	N
R2	2.70 kohms	N	N
R3	0.20 kohms	Y	N
R4	0.20 kohms	Y	N



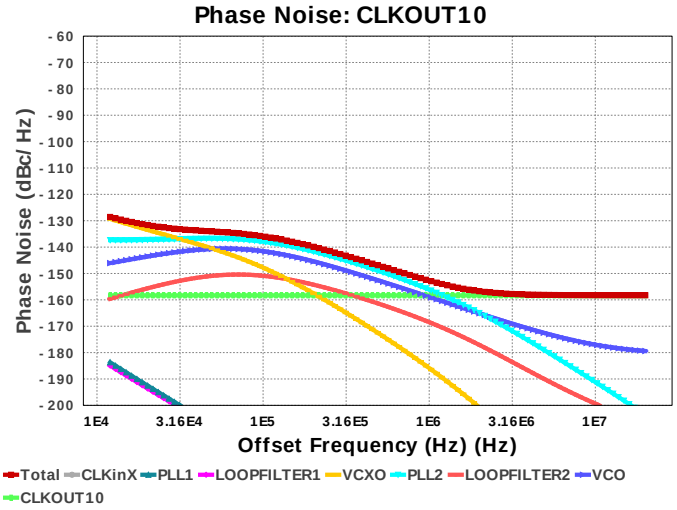
Output Block: LMK04828B_VCO0 LMK04828B_VCO0 : CLKOUT10 as LVDS output, 100.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-152.819 dBc/Hz
RMS Jitter	230.01 fs
RMS Phase Error (deg)	0.008 deg
RMS Phase Error	0.145 mrad
EVM	0.014%
SNR	76.801 dB
Spur	-79.801 dBc
Jitter (Pk-Pk)	1640.085 fs
Jitter (Cycle to Cycle Pk)	3280.169 fs
Jitter (Cycle to Cycle RMS)	325.283 fs
A/D ENOB	12.472 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-128.56	-135.92	-158.27
CLKinX	-205.68	-242.63	-400.24
PLL1	-183.69	-220.94	-378.6
LOOPFILTER1	-184.93	-221.8	-379.41
VCXO	-129.27	-147.77	-259.35
PLL2	-137.36	-137.97	-203.6
LOOPFILTER2	-159.62	-150.88	-207.02
VCO	-146.06	-141.56	-179.4
CLKOUT10	-158.3	-158.3	-158.3



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

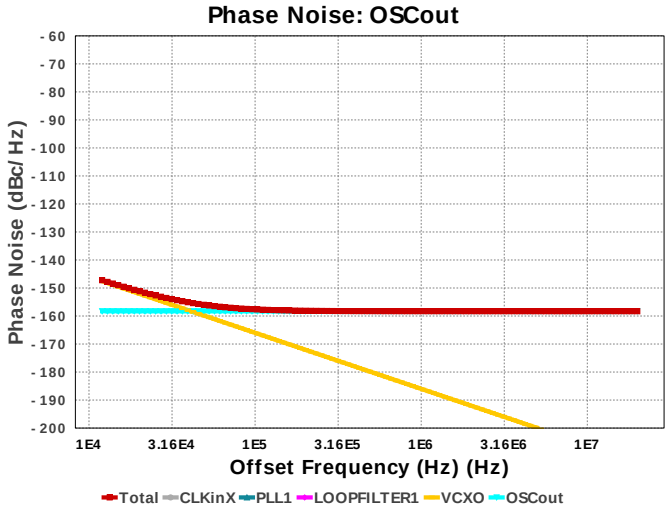
Output Block: LMK04828B_VCO0 LMK04828B_VCO0 : OSCout as LVDS output, 12.5 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-158.269 dBc/Hz
RMS Jitter	982.53 fs
RMS Phase Error (deg)	0.004 deg
RMS Phase Error	0.077 mrad
EVM	0.008%
SNR	82.251 dB
Spur	-85.251 dBc
Jitter (Pk-Pk)	7005.923 fs
Jitter (Cycle to Cycle Pk)	14011.846 fs
Jitter (Cycle to Cycle RMS)	1389.507 fs
A/D ENOB	13.377 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-147.23	-157.62	-158.3
CLKinX	-223.99	-260.86	-352.91
PLL1	-202	-239.16	-331.27
LOOPFILTER1	-203.24	-240.03	-332.08
VCXO	-147.58	-165.99	-212.02
OSCout	-158.3	-158.3	-158.3



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